AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method of fabricating a semiconductor integrated circuit device that has a standby current of 5 μA or below in tests of operation at 90°C and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film ; and

(g) removing that part of said metal film which did not react in step (f).

2. (Cancelled)

3. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

4. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said sputter etching is Ar sputter etching.

5. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said metal film is a film of Co.

6. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said MISFETs configure an SRAM memory cell.

7. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein the metal forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

8. (Previously Presented) A method of fabricating a semiconductor integrated circuit device that has a standby current of 5 μA or below in tests of operation at 90°C and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film , and

(g) removing that part of said metal film which did not react in step (f).

9. (Cancelled)

10. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

11. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said sputter etching is Ar sputter etching.

12. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said metal film is a film of Co.

13. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said MISFETs configure an SRAM memory cell.

14. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

15. (Previously Presented) A method of fabricating a semiconductor integrated circuit device and has MISFETs formed on the main surface of a semiconductor substrate which has a standby current of 1.5 μA or below in actual operation, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film ; and

(g) removing that part of said metal film which did not react in step (f).

16. (Cancelled)

17. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

18. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said sputter etching is Ar sputter etching.

19. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said metal film is a film of Co.

20. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said MISFETs configure an SRAM memory cell.

21. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein the metal forming step is performed,

under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

22. (Previously Presented) A method of fabricating a semiconductor integrated circuit device that has a standby current of 1.5 μA or below in actual operation and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film, and

(g) removing that part of said metal film which did not react in step (f).

23. (Cancelled)

24. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said sputter etching is carried out after

the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

25. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said sputter etching is Ar sputter etching.

26. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said metal film is a film of Co.

27. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said MISFETs configure an SRAM memory cell.

28. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

29. (Previously Presented) A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of semiconductor substrate;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film ; and

(g) removing that part of said metal film which did not react in step (f).

30. (Cancelled)

31. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

32. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said sputter etching is Ar sputter etching.

33. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said metal film is a film of Co.

34. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said MISFETs configure an SRAM memory cell.

35. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

36. (Previously Presented) A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film , and

(g) removing that part of said metal film which did not react in step (f).

37. (Cancelled)

38. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

39. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said sputter etching is Ar sputter etching.

40. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said metal film is a film of Co.

41. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said MISFETs configure an SRAM memory cell.

42. (Previously Presented amended) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

43. (Previously Presented) A method of fabricating a semiconductor integrated circuit device that has MISFETs formed on the main surface of a semiconductor

substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 μm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer with a thickness of 20 to 40 nm where said source/drain regions are in contact with said metallic film , and

(g) removing that part of said metal film which did not react in step (f).

44. (Cancelled)

45. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

46. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said sputter etching is Ar sputter etching.

47. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said metal film is a film of Co.

48. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said MISFETs configure an SRAM memory cell.

49. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

50. (Previously Presented) A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 μm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate and said gate electrode to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer with a thickness of 20 to 40 nm where said

source/drain regions are in contact with said metallic film, and

(g) removing that part of said metal film which did not react in step (f).

51. (Cancelled)

52. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

53. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said sputter etching is Ar sputter etching.

54. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said metal film is a film of Co.

55. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said MISFETs configure an SRAM memory cell.

56. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein the a metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

57. (Previously Presented) A method of fabricating a semiconductor integrated circuit device that has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 μm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer with sheet resistance of 5Ω□ to 12Ω□, where said source/drain regions are in contact with said metal film , and

(g) removing that part of said metal film which did not react in step (f).

58. (Cancelled)

59. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

60. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said sputter etching is Ar sputter etching.

61. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said metal film is a film of Co.

62. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said MISFETs configure an SRAM memory cell.

63. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

64. (Previously Presented) A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 μm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate and on said

gate electrode to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer with sheet resistance of 5Ω□ to 12Ω□, where said source/drain regions are in contact with said metal film, and

(g) removing that part of said metal film which did not react in step (f).

65. (Cancelled)

66. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

67. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said sputter etching is Ar sputter etching.

68. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said metal film is a film of Co.

69. (Original) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said MISFETs configure an SRAM memory cell.

70. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

71. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

($c_1$) forming side walls on side surfaces of said gate electrode; and

($c_2$) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

72. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 71, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

73. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 72, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

74. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said metallic silicide layer has a thickness of 20 to 40 nm.

75. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 74, wherein said metal film is a cobalt film.

76. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

($c_1$) forming side walls on side surfaces of said gate electrode; and

($c_2$) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

77. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 76, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

78. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 77, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

79. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

($c_1$) forming side walls on side surfaces of said gate electrode; and

($c_2$) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

80. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 79, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

81. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 80, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

82. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

($c_1$) forming side walls on side surfaces of said gate electrode; and

($c_2$) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

83. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 82, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

84. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 83, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

85. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method

includes the further steps, between steps (c) and (d), of:

($c_1$) forming side walls on side surfaces of said gate electrode; and

($c_2$) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

86. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 85, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

87. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 86, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

88. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

($c_1$) forming side walls on side surfaces of said gate electrode; and

($c_2$) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions

have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

89. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 88, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

90. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 89, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

91. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

($c_1$) forming side walls on side surfaces of said gate electrode; and

($c_2$) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

92. (Previously Presented) A method of fabricating a semiconductor integrated

circuit device, as claimed in claim 91, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

93. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 92, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

94. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

($c_1$) forming side walls on side surfaces of said gate electrode; and

($c_2$) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

95. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 94, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

96. (Previously Presented) A method of fabricating a semiconductor integrated

circuit device, as defined in claim 95, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

97. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

($c_1$) forming side walls on side surfaces of said gate electrode; and

($c_2$) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

98. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 97, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

99. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 98, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

100. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

($c_1$) forming side walls on side surfaces of said gate electrode; and

($c_2$) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

101. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 100, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

102. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 101, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

103. (Currently Amended) A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a conductive film on said insulating film;

(c) forming semiconductor regions in said semiconductor substrate self-aligned with said conductive film;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate; and

(e) forming silicide layers in said surface of said semiconductor regions and said conductive film,

wherein said semiconductor regions include first semiconductor regions and said insulating film is a first insulating film, and wherein the method further comprises the following steps, between steps (c) and (d), of:

($c_1$) forming second insulating films on side surface of said conductive film; and

($c_2$) forming second semiconductor regions, having a greater impurity concentration than that of said first semiconductor regions, in said semiconductor substrate, self-aligned with said second insulating films, and wherein said silicide layers are formed in said surface of said second semiconductor regions and said conductive film.

104. (Cancelled).

105. (Currently Amended) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103~~104~~, wherein said silicide layers are not in contact with said first semiconductor regions.

106. (Previously Presented) A method of fabricating a semiconductor integrated

circuit device, as defined in claim 105, wherein said silicide layers are positioned such that current leakage between said silicide layers and junctions formed by the first semiconductor regions and said semiconductor substrate is prevented.

107. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

108. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein said sputter etching is Ar sputter etching.

109. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein said silicide layers are cobalt silicide layers.

110. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 109, wherein said cobalt silcide layers in the surface of said second semiconductor regions have a thickness of 20-40 nm.

111. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein the top of the conductive film is also

sputter-etched, to 2.5 nm or less below the surface of the conductive film.

112. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 111, wherein the top of the conductive film is sputter-etched simultaneously with the sputter-etching away the top of said semiconductor substrate.